UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,582	07/29/2002	Kenneth J. Goodnow	15054	5111

23389 7590 05/02/2005

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,582	GOODNOW ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicants' request for reconsideration filed on 1/3/2005 has been reviewed.

2. The amendment filed on 1/3/2005 has been entered, including amended drawings (figures 1, 2), amended specification and amended claims.

3. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Response to Arguments

4. As per claim 4, the applicants contend, "Ornes et al. is directed to way of permitting clock recovery when errors are detected in ECC transmissions in communication lines. Ornes further only teaches checking the integrity of the ECC code itself to determine errors in the ECC codes transmissions themselves. It is not related to optimizing of clock timing signals to ensure maximum data signal transmission/receipt speeds within an IC circuit".

The examiner disagrees and asserts that Tamura et al. teach optimizing of clock timing signals to ensure maximum data signal transmission/receipt speeds within an IC circuit and a data transmission fail point corresponds to a clock speed (described in claim 1 rejection below). Claim 4 is dependent on claim 2 and claim 2 is dependent on claim 1. Ornes wt al. teach an error correction code signal generating circuit for generating error correction code signals according to each data signal transmission, said monitoring circuit comprising an error correction code signal check circuit for receiving said error correction code signals and comparing error correction signals against known error corrections resulting in an error between said error correction code signals and said corresponding known error correction codes (figure 7, 8, col. 8, lines 4-7, lines 22-25, col. 9, lines 13-14, lines 30-34, lines 50-62, Ornes et al.).

Claim Objections

5. Claim 6 is objected to because of the following informalities: In the amendment filed on 1/3/2005, the label Claim 6 (Original) is incorrect. It should be --Claim 6 (Currently Amended)--, as the claim 6 is amended in the amendment filed on 1/3/2005. Appropriate correction is required.

6. Claim 16 is objected to because of the following informalities: In line 5 of claim 16, "adjusting step c)" is incorrect. It should be --adjusting step d)-- as per the amended claim 12. Appropriate correction is required.

Drawings

7. The marked-up copy of amended figure 1 and figure 2 received with the amendment filed on 1/3/2005 is incorrectly labeled as "Replacement Sheet". It should be labeled as "Annotated Sheet". Another Replacement Drawing sheet for figure 1 and figure 2 should be submitted with the drawing changes.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

Replacement Drawing Sheets

Drawing changes must be made by presenting replacement sheets which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments section, or remarks, section of the amendment paper. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). A replacement sheet must include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and within the top margin.

Annotated Drawing Sheets

A marked-up copy of any amended drawing figure, including annotations indicating the changes made, may be submitted or required by the examiner. The annotated drawing sheet(s) must be clearly labeled as "Annotated Sheet" and must be presented in the amendment or remarks section that explains the change(s) to the drawings.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.85(a). Failure to take corrective action within the set period will result in ABANDONMENT of the application.

If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings MUST be filed within the THREE MONTH shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamura et al. (US 6,247,138 B1).

Tamura et al. anticipate claim 1.

Tamura et al. teach a system for dynamically optimizing a clock speed of a clock signal used for timing of data signal transmissions and receptions within an integrated circuit (IC) device comprising: a transmitter means for successively transmitting data signals for receipt by a receiver device within said IC; a clock generator circuit for providing said clock timing signal used for timing said data signal transmission and reception within said IC, each said data signal transmission transmitted at a different clock speed; a monitoring circuit means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and, means for adjusting said clock timing signal according to a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation (figure 2, 11, 33, col. 1, lines 48-54, col. 1, line 66-col. 2, line 9, col. 3, lines 29-57, col. 4, lines 4-10, col. 4, lines 17-32, col. 4, line 65-col. 5, line 5, col. 13, lines 54-58, col. 14, lines 65-67, col. 18, lines 9-16, col. 18, lines 36-62, col. 25, lines 44-49, Tamura et al.).

- Tamura et al. anticipate claim 11.

Tamura et al. teach a method for dynamically optimizing a system clock speed of a clock signal used for timing of data signal transmission and receptions in an Integrated Circuit (IC), said method comprising the steps of: a) successively transmitting data signals for receipt by a receiver device within said IC, b) providing said clock timing signal used for timing of data signal transmission and reception within said IC,

each said data signal transmission transmitted at a different clock speed c) receiving successive data transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed; and, d) adjusting said clock timing signal according to a maximum speed allowed for the IC that avoids said data transmission fail point during real-time operation (figure 2, 11, 33, col. 1, lines 48-54, col. 1, line 66-col. 2, line 9, col. 3, lines 29-57, col. 4, lines 4-10, col. 4, lines 17-32, col. 4, line 65-col. 5, line 5, col. 13, lines 54-58, col. 14, lines 65-67, col. 18, lines 9-16, col. 18, lines 36-62, col. 25, lines 44-49, Tamura et al.).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2, 12, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1) as applied to claim 1 above, and further in view of Rogers (US 5,982,210).

As per claim 2, Tamura et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Tamura et al. do not explicitly teach the specific use of the system wherein said means for adjusting comprises means for generating a feedback control signal for input to said clock generator circuit for adjusting said clock to said maximum speed.

Rogers in an analogous art teaches a high speed system clock generator capable of changing the frequency of its output signal instantaneously when transitioning between different clock speeds (col. 2, lines 41-44, Rogers). Rogers also teaches that during normal operation, the phase locking circuit generates the first clock signal in response to a reference clock signal and a feedback clock signal (figure 2, col. 3, lines 4-6, Rogers).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Rogers by including an additional step of

using the system wherein said means for adjusting comprises means for generating a feedback control signal for input to said clock generator circuit for adjusting said clock to said maximum speed.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to execute high-speed data transmission by changing the clock to the maximum speed.

- As per claim 12, Tamura et al. and Rogers teach the additional limitations.

Rogers teaches teach the method, wherein said adjusting step c) includes the step of generating a feedback control signal for input to said clock generator circuit, said feedback signal for adjusting said clock to said maximum speed (figure 2, col. 2, lines 41-44, col. 3, lines 4-6, Rogers).

- As per claim 18, Tamura et al. and Rogers teach the additional limitations.

Tamura et al. teach the method further including the step of continuously detecting presence of data transmission fail points to ensure that the errors do not occur as the IC incurs different operating conditions, said monitoring including adjusting the clock speed accordingly (col. 4, lines 23-32, Tamura et al.).

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1) as applied to claim 1 above, and further in view of Li et al. (US 5,477,181).
As per claim 3, Tamura et al. substantially teach the claimed invention described in claim 1 (as rejected above).
However Tamura et al. do not explicitly teach the specific use of a clock generator circuit that comprises a multiplexer device comprising one or more clock taps responsive to the feedback control signal for enabling alteration of said clock speed.
Li et al. in an analogous art teach the clock generator that comprises a multiplexer, coupled to said multiphase signal generator, for receiving said plurality of intermediate clock phases and said output control signal and in accordance therewith providing said plurality of additional output clock phases (col. 11, lines 58-63, Li et al.).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Li et al. by including an additional step of

using a clock generator circuit that comprises a multiplexer device comprising one or more clock taps responsive to the feedback control signal for enabling alteration of said clock speed.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a clock generator circuit that comprises a multiplexer device comprising one or more clock taps responsive to the feedback control signal for enabling alteration of said clock speed would provide the opportunity to frequency divide clock signals using the control signal.

13. Claims 4, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1) and Rogers (US 5,982,210) as applied to claim 2 above, and further in view of Ornes et al. (US 6,748,567 B1).

As per claim 4, Tamura et al. and Rogers substantially teach the claimed invention described in claim 2 (as rejected above). Tamura et al. also teach a data transmission fail point corresponds to a clock speed resulting in an error corresponding to each data transmission (col. 4, lines 31-33, Tamura et al.). However Tamura et al. and Rogers do not explicitly teach the specific use of an error correction code signal generating circuit for generating error correction code signals according to each data signal transmission, said monitoring circuit comprising an error correction code signal check circuit for receiving said error correction code signals and comparing error correction signals generated against known error corrections, resulting in an error between said error correction code signals and said corresponding known error correction codes.

Ornes et al. in an analogous art teach an embodiment of a method and system is disclosed that provides a reliable ECC code that is transmitted as part of a serial stream (col. 2, lines 52-54, Ornes et al.). Ornes wt al. also teach that after all of the data to be covered by the ECC code has been communicated to the base code generator 714, the base code generator completes generation of the base ECC code. The resulting 10-bit characters representing the ECC code are communicated to register 710 and finally to FIFO 712, from which they will be serially transmitted (figure 7, col. 8, lines 4-7, lines 22-25, Ornes et al.). Ornes et al. teach that FIG. 8 shows a receiving system 800 in accordance with an embodiment of the invention. Base code generator generates an expected base ECC code based on the

10-bit data received in the transmitted cell. The base code generator 812 will generate the expected base ECC code in a manner similar to that done by the transmit system, e.g., using the system shown in FIG. 6. Once the transmitted ECC code has been converted back to two 6-bit characters, in one embodiment, then a comparison between the actual transmitted ECC code and the newly generated expected ECC code is made using XOR logic 824. The two codes are bitwise XORed, resulting in a generated syndrome (every compared bit that does not match will generate a logical "1" and every match will generate a logical "0"). The ECC syndrome indicates, when non-zero, what bit in the data must be flipped to correct a single-bit error. If the ECC syndrome is zero, no error has been detected, and the data will be read from the ECC FIFO without any correction. But if the ECC syndrome is non-zero, correction will be attempted (figure 8, col. 9, lines 13-14, lines 30-34, lines 50-62, Ornes et al.).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Ornes et al. by including an additional step of using an error correction code signal generating circuit for generating error correction code signals according to each data signal transmission, said monitoring circuit comprising an error correction code signal check circuit for receiving said error correction code signals and comparing error correction signals generated against known error corrections, resulting in an error between said error correction code signals and said corresponding known error correction codes.
This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if the transmitted data is received correctly by the receiver and if there is an error in the received data, error correction will be attempted.

- As per claim 13, Tamura et al., Rogers and Ornes et al. teach the additional limitations.

Ornes et al. teach the method, further comprising the steps of: generating error correction code signals according to each data signal transmission, receiving said error correction code signals and comparing error correction signals generated at each clock speed against known error correction codes corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock

speed resulting in an error between said error correction signals and said corresponding known error correction codes (figure 8, col. 9, lines 13-14, lines 30-34, lines 50-62, Ornes et al.).

14. Claims 5, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1) and Rogers (US 5,982,210) as applied to claim 2 above, and further in view of Mergenthaler et al. (US 4,070,648).

As per claim 5, Tamura et al. and Rogers substantially teach the claimed invention described in claim 2 (as rejected above). Tamura et al. also teach a means for delaying each of a series of data transmission signals generated at different clock speeds (col. 4, lines 61-64, Tamura et al.). Tamura et al. teach a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission (col. 2, lines 2-5, col. 4, lines 30-32, Tamura et al.). Tamura et al. also teach delayed data transmission signals (col. 4, lines 60-61, Tamura et al.).

However Tamura et al. and Rogers do not explicitly teach the specific use of the monitoring circuit comprising an error check circuit for receiving each of said series of data transmission signals and comparing each data transmission signal against a corresponding known data signal transmission. Mergenthaler et al. in an analogous art teach that as each bit of data message is transmitted ... altered the data (col. 4, lines 19-28, Mergenthaler et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Mergenthaler et al. by including an additional step of using the monitoring circuit comprising an error check circuit for receiving each of said series of data transmission signals and comparing each data transmission signal against a corresponding known data signal transmission.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine if the transmitted data is received correctly by the receiver.

- As per claim 14, Tamura et al. also teach delaying each of a series of data transmission signals generated at different clock speeds (col. 4, lines 61-64, Tamura et al.). Tamura et al. teach a data

transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission (col. 2, lines 2-5, col. 4, lines 30-32, Tamura et al.). Tamura et al. also teach delayed data transmission signals (col. 4, lines 60-61, Tamura et al.).

Mergenthaler et al. teach receiving each of said series of data transmission signals and comparing each data transmission signal against its corresponding known data transmission (col. 4, lines 19-28, Mergenthaler et al.).

15. Claims 6, 7, 8, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1) and Rogers (US 5,982,210) as applied to claim 2 above, and further in view of Kundu et al. (US 6,510,398 B1).

As per claim 6, Tamura et al. and Rogers substantially teach the claimed invention described in claim 2 (as rejected above). Tamura et al. also teach a data transmission fail point corresponds to a clock speed (col. 2, lines 2-4, col. 4, lines 30-32, Tamura et al.).

However Tamura et al. and Rogers do not explicitly teach the specific use of the system comprising: a random data generating circuit for generating unique random data signals for transmission throughout a data path of a circuit within said IC device, said circuit for processing said random data signals and generating a corresponding data output; said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit to determine an error between said generated random data and said corresponding processing circuit output.

Kundu et al. in an analogous art teach that FIG. 1 ... the DUT (fig. 1, col. 3, lines 42-46, Kundu et al.). Kundu et al. also teach that the next action 130 ... the test result (col. 3, line 66-col. 4, line 6, Kundu et al.). Kundu et al. teach that action 180 ... test result (col. 4, lines 32-33, Kundu et al.). Kundu et al. teach that FIG. 2 ... random data pattern (fig. 2, col. 4, lines 43-50, Kundu et al.). Kundu et al. also teach including the pattern generator in the integrated circuit (col. 4, line 62, Kundu et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Kundu et al. by including an additional step of using the system comprising: a random data generating circuit for generating unique random data signals

for transmission throughout a data path of a circuit within said IC device, said circuit for processing said random data signals and generating a corresponding data output; said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit for an error between said generated random data and said corresponding processing circuit output.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect an error in an integrated circuit device circuit.

- As per claim 7, Tamura et al., Rogers and Kundu et al. teach the additional limitations.

Kundu et al. teach the system wherein the comparator means generates the feedback control signal indicating said data output of said processing circuit matches said generated random data (figure 1, 2, col. 3, line 66-col. 4, line 6, col. 4, lines 32-33, col. 4, lines 40-50, Kundu et al.).

Rogers teaches that the feedback control signal is input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be increased (figure 2, col. 2, lines 41-44, col. 3, lines 4-6, Rogers).

- As per claim 8, Tamura et al., Rogers and Kundu et al. teach the additional limitations.

Kundu et al. teach the system wherein the comparator means generates said feedback control signal indicating said data output of said processing circuit does not match said generated random data (figure 1, 2, col. 3, line 66-col. 4, line 6, col. 4, lines 32-33, col. 4, lines 40-50, Kundu et al.).

Rogers teaches that the feedback control signal is input to the clock generator circuit for enabling the clock frequency provided by clock generator circuit to be decreased (figure 2, col. 2, lines 41-44, col. 3, lines 4-6, Rogers).

- As per claim 15, Tamura et al., Rogers and Kundu et al. teach the additional limitations.

Tamura et al. also teach a data transmission fail point corresponds to a clock speed (col. 2, lines 2-4, col. 4, lines 30-32, Tamura et al.).

Kundu et al. teach generating unique random data transmission signals; transmitting said unique random data signals throughout a data path of a circuit within said IC device for processing therein, and

generating a corresponding data output signal; and comparing said generated random data against said corresponding data output of said processing circuit to determine an error between said generated random data and said corresponding processing circuit output (fig. 1, fig. 2, col. 3, lines 42-46, col. 3, line 66-col. 4, line 6, col. 4, lines 32-33, col. 4, lines 43-50, col. 4, line 62, Kundu et al.).

- As per claim 16, Tamura et al., Rogers and Kundu et al. teach the additional limitations.

Kundu et al. teach the method wherein said feedback control signal includes a first signal indicating a match between said data output signal of said data path and said generated unique random data, or generating a second output signal indicating no match between said data output signal of said data path and said generated unique random data (figure 1, 2, col. 3, line 66-col. 4, line 6, col. 4, lines 32-33, col. 4, lines 40-50, Kundu et al.).

Rogers teaches that adjusting step d) includes responding to either said first or second output signals for respectively increasing or decreasing a clock frequency of said clock signal (figure 2, col. 2, lines 41-44, col. 3, lines 4-6, Rogers).

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1), Rogers (US 5,982,210) and Kundu et al. (US 6,510,398 B1) as applied to claim 6 above, and further in view of Collier (US 2002/0107897 A1).

As per claim 9, Tamura et al., Rogers and Kundu et al. substantially teach the claimed invention described in claim 6 (as rejected above).

However Tamura et al., Rogers and Kundu et al. do not explicitly teach the specific use of the system, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

Collier in an analogous art teaches that when a call for random data is received at input 6 by the random number generator 1 the processing means 2 performs a series of processing steps as described below to generate a random number. The random number is then output by the random number generator at output 7. When the random number generator is called the processing means is arranged to access a seed value stored in temporary store 5, perform an algorithm which takes the seed value as input and

based on that seed value to generate random data and a seed value which is stored for use by the next iteration of the algorithm (figure 1, page 2, paragraph 16, Collier).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Collier by including an additional step of using the system, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate random data that can be used for testing different parameters of a circuit.

17. Claims 10, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura et al. (US 6,247,138 B1), Rogers (US 5,982,210) and Mergenthaler et al. (US 4,070,648) as applied to claim 5 above, and further in view of Tada et al. (US 2001/0047319 A1).

As per claim 10, Tamura et al., Rogers and Mergenthaler et al. substantially teach the claimed invention described in claim 5 (as rejected above). Mergenthaler et al. also teach the error check circuit (item 224 in fig. 3, col. 4, lines 23-26, Mergenthaler et al.).

However Tamura et al., Rogers and Mergenthaler et al. do not explicitly teach the specific use of the system, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals.

Tada et al. in an analogous art teach that when a load on a communication line is increased, a delay occurs in operation of a program used by the transmitting server, which delivers data to the receiving servers (page 1, paragraph 8, Tada et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tamura et al.'s patent with the teachings of Tada et al. by including an additional step of using the system, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to verify the data received by the receiver for errors.

- As per claim 17, Tamura et al., Rogers and Mergenthaler et al. and Tada et al. teach the additional limitations.

Tada et al. teach the method, wherein said delaying step includes the step of increasing a load applied to data lines carrying said data transmission signals (page 1, paragraph 8, Tada et al.).

Mergenthaler et al. teach the error check circuit (item 224 in fig. 3, col. 4, lines 23-26, Mergenthaler et al.).

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

GUY LAMARRE
PRIMARY EXAMINER